QualityThought®
Transforming Dreams! Redefining Future!

CELEBRATING 15 YEARS

BENEFITS OF LEARNING

VLSI

(Very Large Scale Integration)

For More Details 91211 88426

Introduction To VLSI

- What Is Vlsi ? Evolution Of Vlsi
- Vlsi Design Flow Overview
- Moore's Law And Scaling Trends
- Asic Vs Fpga
- Applications Of Vlsi In Real Life

Digital Electronics

- Number Systems , Conversions
- Logic Gates,boolean Algebra, Minimization Techniques (k-maps)
- Combinational Circuits : Adders, Mux, Encoders,decoders, Comparators
- Sequential Circuits : Latches, Flipflops,registers,shift Registers
- Fsms : Moore And Melay Machines

Verilog HDL

- Verilog Syntax: Modules,ports,nets,registers
- Modeling Styles: Behavioral,dataflow,structural
- Procedural Blocks : Always,initial, Blocking/non-blocking
- Tasks And Functions, Parameterization,fork Join
- Design Hierarchy And Testbenches
- Simulation With Eda Playground And Modelsim

SYSTEM VERILOG

- Data Types: Logic,bit,arrays,packed/unpacked
- Interfaces,fork Join None, Fork Join Any
- Randomization,constraints,for Each Loops
- System Verilog Assertions(sva): Immediate And Concurrent
- Functional Coverage: Coverpoints,cross Coverage
- Testbench Architecture

UVM

- Introduction To Verification Methodologies – Uvm
- Verification Planning And Testbench Architectrure
- Uvm Overview : Components

Debugging in C#

- Various Types of .NET Projects
- Tracing, Debugging, Build
- Compile Options
- Using break points
- Using break conditions
- Debugging Exception
- Using watch and output window
- What are Diagnostics?
- Debug and Trace Classes
- Creating multiple projects within one solution
- Customizing Visual Studio Settings – Extensions, NUGet Package, Environmental Settings
- Using watch and output window
- Creating multiple projects within one solution
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